

CLAIMS

- 1 1. A semiconductor structure comprising:
2 a semiconductor substrate;
3 at least one first crystalline epitaxial layer on said substrate, said first layer having a
4 surface which is planarized; and
5 at least one second crystalline epitaxial layer on said at least one first layer.

- 1 2. The structure of claim 1, wherein said at least one first crystalline epitaxial layer is
2 lattice mismatched.

- 1 3. The structure of claim 1, wherein said at least one second crystalline epitaxial layer
2 is lattice mismatched.

- 1 4. The structure of claim 1, wherein said first and second crystalline epitaxial layers
2 are lattice mismatched.

- 1 5. The structure of claims 2, wherein said at least one first layer comprises a
2 composition graded relaxed epitaxial region.

- 1 6. The structure of claims 3, wherein said at least one second layer comprises a
2 composition graded relaxed epitaxial region.

1 7. The structure of claims 4, wherein said first and second layers comprise
2 composition graded relaxed epitaxial regions.

1 8. The structure of claim 7, wherein said at least one first layer comprises a first
2 composition graded relaxed epitaxial region and a first uniform composition layer.

1 9. The structure of claim 8, wherein said at least one second layer comprises a second
2 uniform composition layer and a second composition graded relaxed epitaxial region.

1 10. The structure of claim 9, wherein said first and second uniform composition layers
2 are substantially lattice mismatched.

1 11. The structure of claim 9, wherein the surface of said at least one second layer
2 comprises substantially fewer threading dislocations and dislocation pile-ups.

1 12. The structure of claim 9, wherein said substrate comprises silicon, and said first
2 and second composition graded relaxed epitaxial regions and said first and second uniform
3 composition layers comprise a $\text{Ge}_x\text{Si}_{1-x}$ alloy.

1 13. The structure of claim 12, wherein the planarization occurs at a composition of
2 approximately 50%.

1 14. The structure of claim 13, wherein the final Ge concentration is approximately
2 between 70 and 100%.

1 15. The structure of claims 1, wherein said at least one second crystalline epitaxial
2 layer comprises a surface which is planarized.

1 16. The structure of claim 15, wherein subsequent epitaxial layers are provided on said
2 second layer, each of which comprises a surface which is planarized.

1 17. The structure of claim 1, wherein said first layer is planarized by chemical-
2 mechanical polishing.

1 18. The structure of claim 15, wherein a first planarization occurs at approximately
2 between 20 and 35% GeSi, and a second planarization occurs at approximately between 50 and
3 70% GeSi.

1 19. The structure of claim 12, wherein compressive strain is incorporated in said
2 graded region to offset the tensile strain that is incorporated during thermal processing.

1 20. The structure of claim 1, wherein alloys of $\text{Ge}_x\text{Si}_{1-x}$ from $x=0$ to about $x\approx 35\%$ are
2 grown at 750°C , alloys from $x=35$ to about $x\approx 75\%$ are grown at between 650°C and 750°C ,
3 and alloys greater than 75% are grown at 550°C .

1 21. A semiconductor structure comprising:

2 a silicon substrate; and

3 a GeSi graded region grown on said silicon substrate, compressive strain being
4 incorporated in said graded region to offset the tensile strain that is incorporated during
5 thermal processing.

1 22. The structure of claim 21, wherein the compressive strain is incorporated by
2 growing GeSi alloys at lower temperatures such that the alloy does not completely relax.

1 23. The structure of claim 21, wherein the compressive strain is incorporated by
2 decreasing the growth temperature as Ge concentration increases in said graded region.

1 24. The structure of claim 21, wherein alloys of $\text{Ge}_x\text{Si}_{1-x}$ from $x=0$ to about $x\approx 35\%$
2 are grown at 750°C , alloys from $x=35$ to about $x\approx 75\%$ are grown at between 650°C and
3 750°C , and alloys greater than 75% are grown at 550°C .

1 25. The structure of claim 21, wherein said graded region comprises a surface which is
2 planarized.

1 26. The structure of claim 25, wherein said graded region is planarized by chemical-
2 mechanical polishing.

1 27. A semiconductor structure comprising:
2 a semiconductor substrate;
3 a first layer having a graded region grown on said substrate, compressive strain being
4 incorporated in said graded region to offset the tensile strain that is incorporated during
5 thermal processing, said first layer having a surface which is planarized; and
6 a second layer provided on said first layer.

1 28. A method of fabricating a semiconductor structure comprising:
2 providing a semiconductor substrate;
3 providing at least one first crystalline epitaxial layer on said substrate; and
4 planarizing the surface of said first layer.

1 29. The method of claim 28 further comprising providing at least one second
2 crystalline epitaxial layer on said first layer.

1 30. The method of claim 28, wherein said step of providing said first layer comprises
2 growing a GeSi relaxed graded region on said substrate.

1 31. The method of claim 30 further comprising incorporating compressive strain in
2 said grade region to offset tensile strain incorporated during thermal processing.

1 32. The method of claim 31, wherein said step of incorporating compressive strain
2 comprises decreasing the growth temperature as Ge concentration increases in said graded
3 region.

1 33. The method of claim 32, wherein said step of incorporating compressive strain
2 comprises growing alloys of $\text{Ge}_x\text{Si}_{1-x}$ from $x=0$ to about $x\approx 35\%$ at 750°C , growing alloys
3 from $x=35$ to about $x\approx 75\%$ at between 650°C and 750°C , and growing alloys greater than
4 75% at 550°C .

1 34. The method of claim 28, wherein said step of planarizing comprises chemical-
2 mechanical polishing.